Elektronische Bauelemente

SPWNE555D

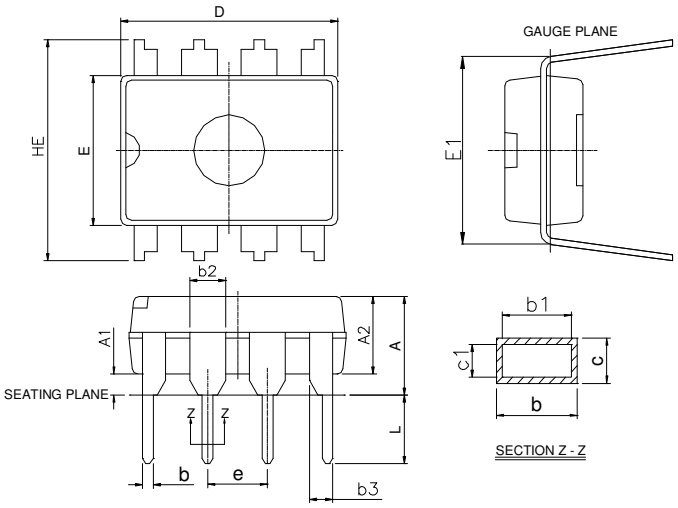
Single Timer

RoHS Compliant Product

DIP-8

Description

The SPWNE555D is a highly stable timer integrated circuit. It can be operated in Astable mode and Monostable mode. With monostable operation, the time delay is controlled by one external and one capacitor. With a stable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

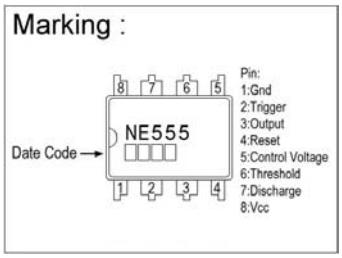


Features

* Turn Off Time Less Than 2uSec
* Adjustable Duty Cycle
* Timing From uSec to Hours
* High Current Driver Capability (=200mA)

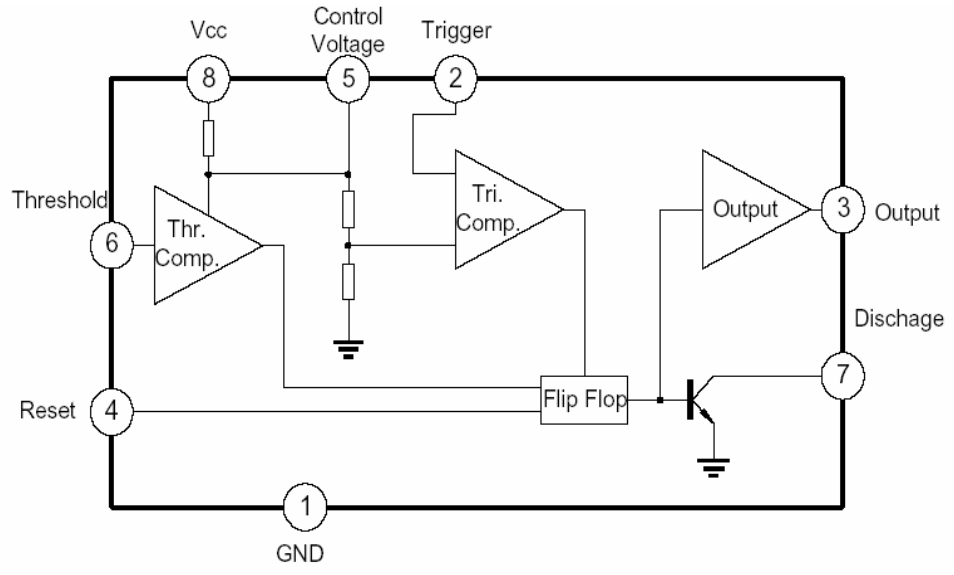
Applications

* Time Delay Generation
* Pulse Generation
* Precistion Timing



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	-	0.5334	c1	0.203	0.279
A1	0.381	-	D	9.017	10.16
A2	2.921	4.953	E	6.096	7.112
b	0.356	0.559	E1	7.620	8.255
b1	0.356	0.508	e	2.540 BSC	
b2	1.143	1.778	HE	-	10.92
b3	0.762	1.143	L	2.921	3.810
c	0.203	0.356			

Block Diagram & Pin Configuration



Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Current	I_O	200	mA
Power Dissipation	Pd	600	mW
Lead Temperature (10sec)	Tlead	300	℃
Operating Temperature	Topr	0 ~ 70	℃
Storage Temperature	Tstg	-65 ~ 150	℃

Electrical Characteristics (T_A=25℃ V_{CC}=5 ~ 15V)

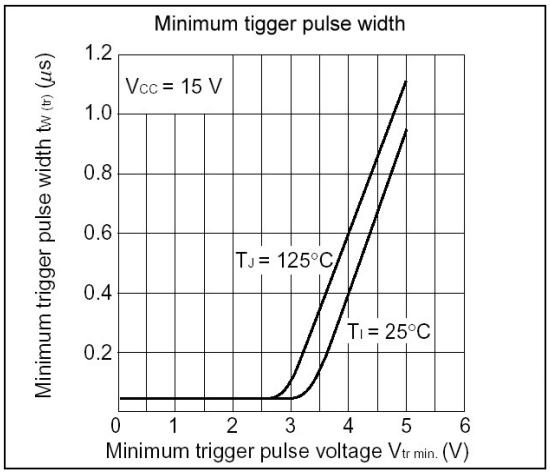
Parameter	Symbol	Test Conditions	Min	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.5	-	16	V
Supply Current (Note 1)	I_{CC}	V_{CC}=5V, RL=∞	-	3	6	mA
		V_{CC}=15V, RL=∞	-	10	15	mA
Timing Error(monostable)						
Initial Accurary (Note 1)	ACCUR	R_A=1k to 100kΩ	-	1.0	-	%
Drift with Temperature	△t/△T	C=0.1μF	-	50	-	ppm/℃
Drift with Supply Voltage	△t/△V_{CC}		-	0.1	-	%/V
Timing Error(astable)						
Initial Accurary (Note 1)	ACCUR	R_A=1k to 100kΩ	-	2.25	-	%
Drift with Temperature	△t/△T	C=0.1μF	-	150	-	ppm/℃
Drift with Supply Voltage	△t/△V_{CC}		-	0.3	-	%/V
Control Voltage	V_C	V_{CC}=15V	9.0	10.0	11.0	V
		V_{CC}=5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC}=15V	9.2	10.0	10.8	V
		V_{CC}=5V	3.1	3.33	3.55	V
Threshold Current (Note 3)	I_{TH}		-	0.1	0.25	μA
Trigger Voltage	V_{tr}	V_{CC}=5V	1.1	1.67	2.2	V
		V_{CC}=15V	4.5	5	5.6	V
Trigger Current	I_{tr}	V_{tr}=0	-	-	2.0	μA
Reset Voltage	V_{rst}		0.4	0.7	1.0	V
Reset Current	I_{rst}		-	0.1	0.4	mA
Low Output Voltage	V_{OL}	V_{CC}=15V, I_{sink}=10mA	-	0.06	0.25	V
		V_{CC}=15V, I_{sink}=50mA	-	0.3	0.75	
		V_{CC}=5V, I_{sink}=5mA	-	0.05	0.35	
High Output Voltage	V_{OH}	V_{CC}=15V, I_{sink}=200mA	-	12.5	-	V
		V_{CC}=15V, I_{sink}=100mA	12.75	13.3	15	
		V_{CC}=5V, I_{sink}=100mA	2.75	3.3	5	
Reset Time of Output	t_R		-	100	-	nSec
Fall Time of Output	t_F		-	100	-	nSec
Discharge leakage Current	I_{LKG}		-	20	100	nA

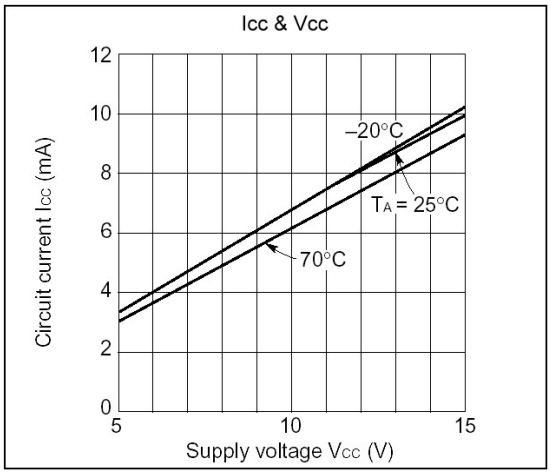
Note1: Supply current when output is high typically 1mA less at V_{CC}=5V.

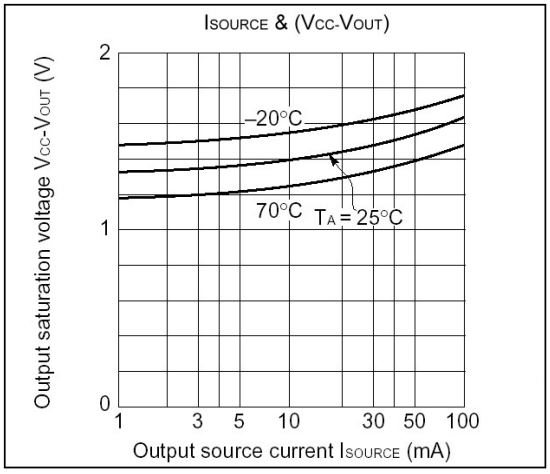
Note2: Tested at V_{CC}=5V and V_{CC}=15V.

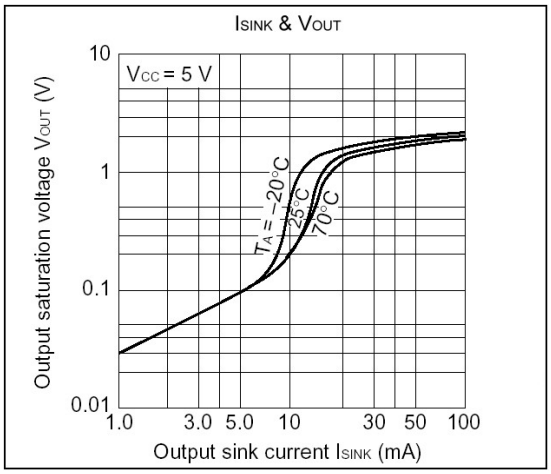
Note3: This will determine the maximum value of RA+RB for 15V operation, the maximum total is R=20MΩ, and for 5V operation the maximum total is R=6.7MΩ.

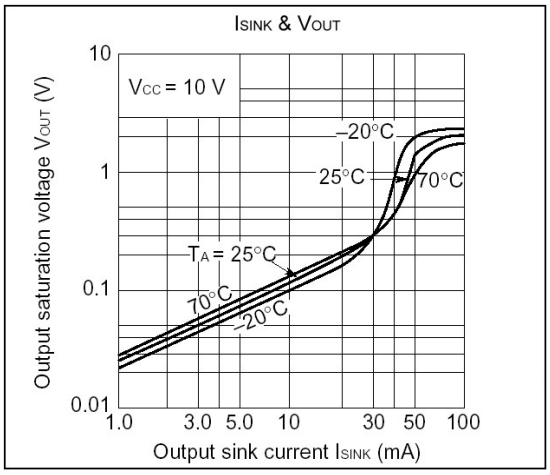
Characteristics Curve

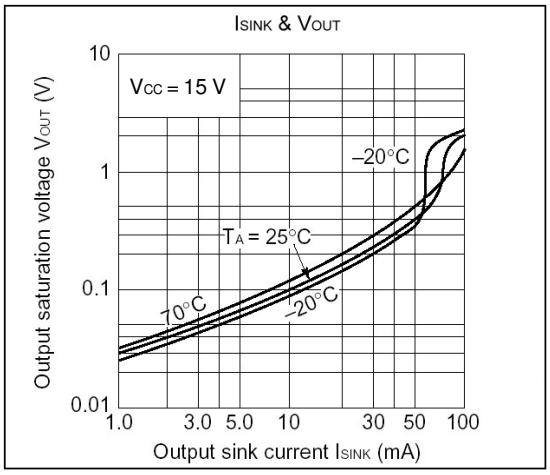


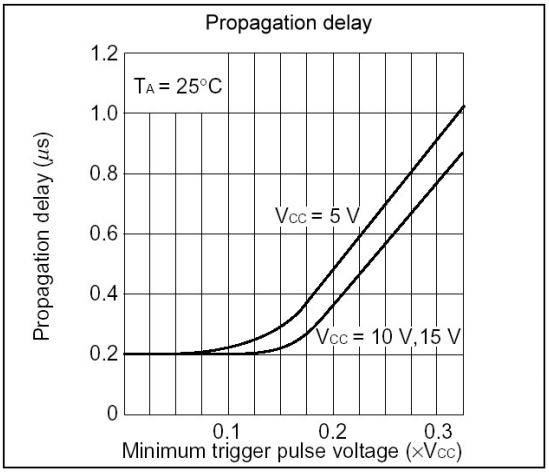


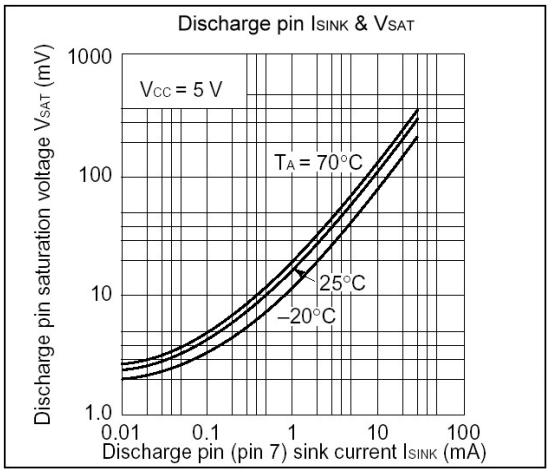


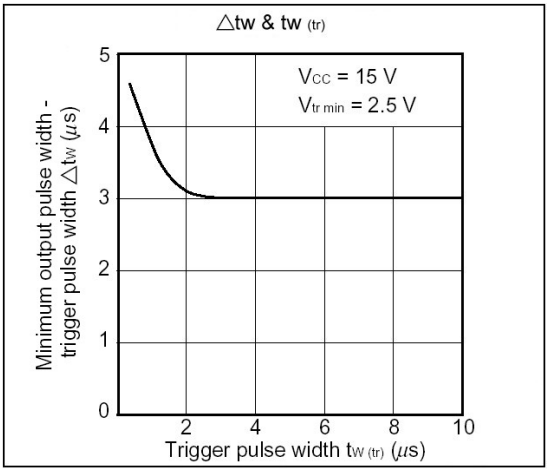


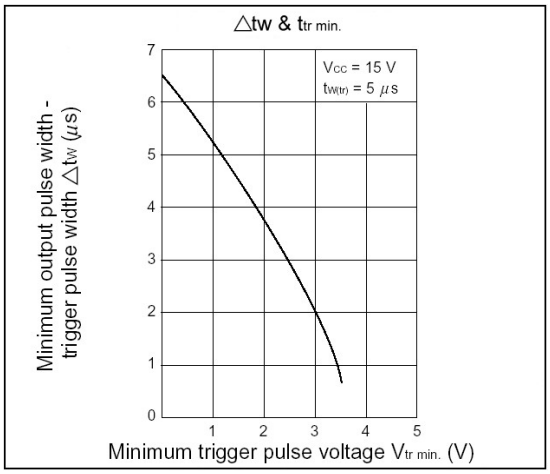




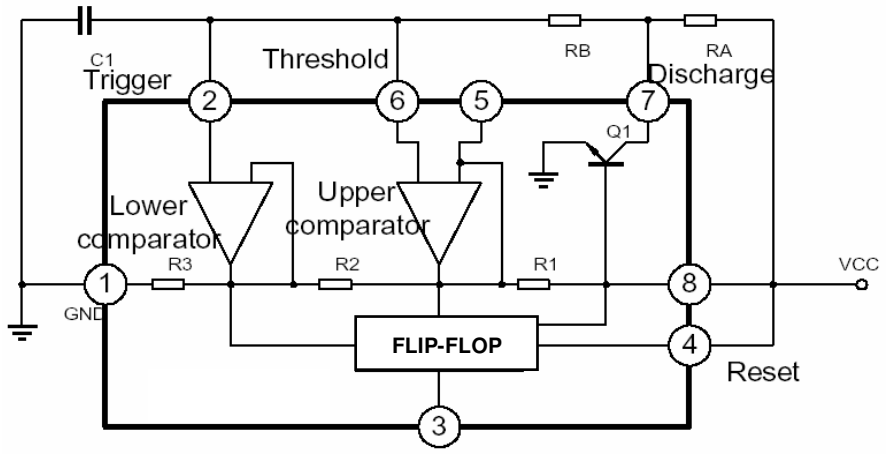

Propagation delay
Propagation delay (μs)
1.2
1.0
0.8
0.6
0.4
0.2
0
TA = 25°C
VCC = 5 V
VCC = 10 V,15 V
0.1
0.2
0.3
Minimum trigger pulse voltage (×VCC)


Discharge pin ISINK & VSAT
Discharge pin saturation voltage VSAT (mV)
1000
100
10
1.0
VCC = 5 V
TA = 70°C
25°C
–20°C
0.01
0.1
1
10
100
Discharge pin (pin 7) sink current ISINK (mA)


△tw & tw (tr)
Minimum output pulse width - trigger pulse width △tW (μs)
5
4
3
2
1
0
VCC = 15 V
Vtr min = 2.5 V
2
4
6
8
10
Trigger pulse width tW (tr) (μs)


△tw & ttr min.
Minimum output pulse width - trigger pulse width △tW (μs)
7
6
5
4
3
2
1
0
VCC = 15 V
tW(tr) = 5 μs
1
2
3
4
5
Minimum trigger pulse voltage Vtr min. (V)

Application Circuit



Application Notes

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (Reset) is tied to V_{CC} (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA, RB and discharge through RB only. In the internal circuit of SPWNE555D, one input of the upper comparator is at voltage of $2/3V_{CC}$ ($R1=R2=R3$), another input is connected to Pin 6. As soon as C1 is charging to higher than $2/3V_{CC}$, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of $1/3V_{CC}$, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, flip-flop circuit is set output high.

That is, when C1 charges through RA and RB, output is high and when C1 discharge through RB, output is low. The charge time (output is high) t1 is 0.693 (RA+RB) C1 and the discharge time (output is low) T2 is 0.693RB*C1.

$$\ln\left(\frac{Vcc-\frac{1}{3}Vcc}{Vcc-\frac{2}{3}Vcc}\right)=0.693$$

$T1=0.693*(RA+RB)*C1$

Thus the total period time T is given by $T2=0.693*RB*C1$

$T=T1+T2=0.693(RA+2RB)*C1.$

Then the frequency of astable mode is given by

$$f=\frac{1}{T}=\frac{1.44}{(RA+2RB)*C1}$$

The duty cycle is given by

$$D.C.=\frac{T2}{T}=\frac{RB}{RA+2RB}\ .$$